http://www.analog.com/zh/circuits-from-the-lab/CN0270/vc.html

Devices Connected/Referenced

连接/参考器件

AD5700, AD5700-1 Low Power HART® Modem AD5420 16-Bit 4 mA to 20 mA DAC

AD5700、AD5700-1 低功耗 HART®调制解调器 AD5420 16 位 4 mA 至 20 mA DAC

Complete 4 mA to 20 mA HART Solution

完整的4 mA至20 mA HART解决方案

EVALUATION AND DESIGN SUPPORT

评估和设计支持

Circuit Evaluation Boards

电路评估板

AD5420 Circuit Evaluation Board (EVAL-AD5420EBZ)

AD5420电路评估板(EVAL-AD5420EBZ)

AD5700-1/AD5700 Evaluation Board (EVAL-AD5700-1EBZ)

AD5700-1/AD5700评估板(EVAL-AD5700-1EBZ)

Design and Integration Files

设计和集成文件

Schematics, Layout Files, Bill of Materials

原理图、布局文件、物料清单

CIRCUIT FUNCTION AND BENEFITS

电路功能与优势

The circuit shown in Figure 1 uses the AD5700, the industry's lowest power and smallest footprint HART[1]-compliant IC modem and the AD5420, a 16-bit current-output DAC, to form a complete HART-compatible 4 mA to 20 mA solution.

图 1 所示的电路使用 AD5700——低功耗，小尺寸的 HART[1] 兼容型 IC 调制解调器，以及 AD5420 16 位电流输出 DAC，形成完整的 HART 兼容型 4 mA 至 20 mA 解决方案。

For additional space savings, the AD5700-1 offers a 0.5% precision internal oscillator.

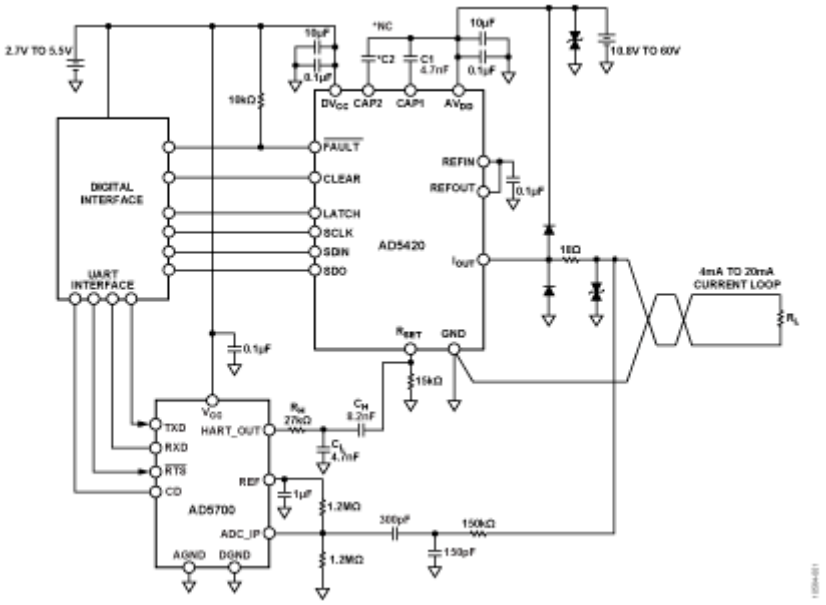
为了进一步节省空间，AD5700-1 提供了精度为 0.5%的内部振荡器。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 1. AD5420 HART-ENABLED CIRCUIT SIMPLIFIED SCHEMATIC

图 1. AD5420 HART 使能电路简化原理图



Enlarge

放大

This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation, for example, the analog rate of change and noise during silence specifications.

该电路符合由 HART 通信基金会定义的 HART 物理层规范，例如模拟变化率和静默期间噪声规格。

For many years, 4 mA to 20 mA communication has been used in process control instrumentation. This communication method is reliable and robust, and offers high immunity to environmental interference over long communication distances. A limitation, however, is that only 1-way communication of one process variable at a time is possible.

多年来，过程控制仪器仪表中一直使用 4 mA 至 20 mA 通信。此通信方式稳定可靠，对长距离通信中的环境干扰具有高抗扰度。不过，其限制是每次只能进行一个过程变量的单向通信。

The development of the highway addressable remote transducer (HART) standard provided highly capable 2-way digital communication, simultaneously with the 4 mA to 20 mA analog signaling used by traditional instrumentation equipment. This allows for features such as remote calibration, fault interrogation, and transmission of additional process variables. Put simply, HART is a digital two-way communication in which a 1 mA peak-to-peak frequency-shift-keyed (FSK) signal is modulated on top of the 4 mA to 20 mA analog current signal.

可寻址远程传感器高速通道(HART)标准的开发实现了高性能的双向数字通信，同时支持传统仪器仪表设备所使用的 4 mA 至 20 mA 模拟信号。它衍生出各种特性，例如远程校准、故障查询和额外过程变量的传输。简言之，HART 是一种数字双向通信系统，其在 4 mA 至 20 mA 模拟电流信号之上调制一个 1 mA p-p 频移键控(FSK)信号。

back to top

返回页首

CIRCUIT DESCRIPTION

电路描述

Figure 1 shows the manner in which the AD5420 can be combined with the AD5700 HART modem and a UART interface to construct a HART-capable 4 mA to 20 mA current output, typical of PLC and DCS systems. The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the R_{SET} pin of the AD5420. If the external R_{SET} resistor is not being used, an alternative method of connecting the AD5420 and the AD5700 can be found in Application Note AN-1065, where the AD5700 HART modem output is coupled into the AD5420 via the CAP2 pin. While the method described in this circuit note requires the use of the external RSET resistor, it provides better power supply rejection performance than the alternative application note solution. The use of either solution results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current (as shown in Figure 2) without affecting the dc level of the current. The diode protection circuitry (D1 − D4) is discussed in more detail in the Transient Voltage Protection section.

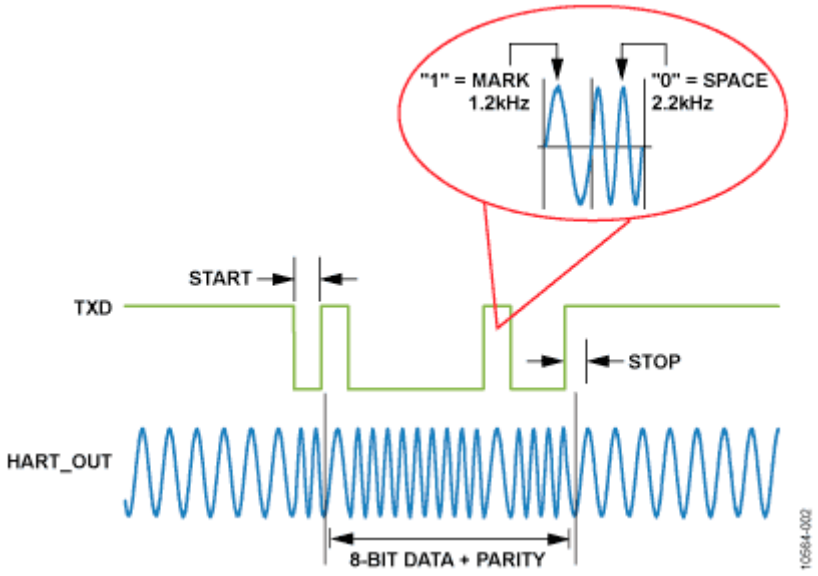
图 1 显示 AD5420 如何与 AD5700 HART 调制解调器和 UART 接口配合使用，以使 PLC 和 DCS 系统常用的 4 mA 至 20 mA 电流输出支持 HART。从 AD5700 输出的 HART_OUT 信号经过衰减后，交流耦合至 AD5420 的 R_{SET} 引脚。如果未使用外部 R_{SET} 电阻，连接 AD5420 和 AD5700 的替代方法请参见应用笔记 AN-1065，其中 AD5700 HART 调制解调器输出通过 CAP2 引脚耦合到 AD5420。虽然本电路笔记中所述的方法需要使用外部 RSET 电阻，但电源抑制性能却高于替代应用笔记解决方案。无论使用哪一种解决方案，AD5700 HART 调制解调器输出均可在不影响电流直流电平的前提下调制 4 mA 至 20 mA 模拟电流（如图 2 所示）。二极管保护电路(D1 − D4)将在瞬变电压保护部分详细论述。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 2. AD5700/AD5700-1 SAMPLE MODULATOR WAVEFORM

图 2. AD5700/AD5700-1 样片调制器波形



Enlarge

放大

Determining the Values of the External Components

确定外部元件值

C1 and C2 can be used in conjunction with the digital slew rate control functionality of the part to control the slew rate of the IOUT signal of the AD5420. In determining the absolute values of the capacitors, ensure that the FSK output from the modem is passed undistorted. Thus, the bandwidth presented to the modem output signal must pass the 1200 Hz and 2200 Hz frequencies. Figure 3 shows a circuit that achieves this requirement. In this case, C2 is left open-circuit.

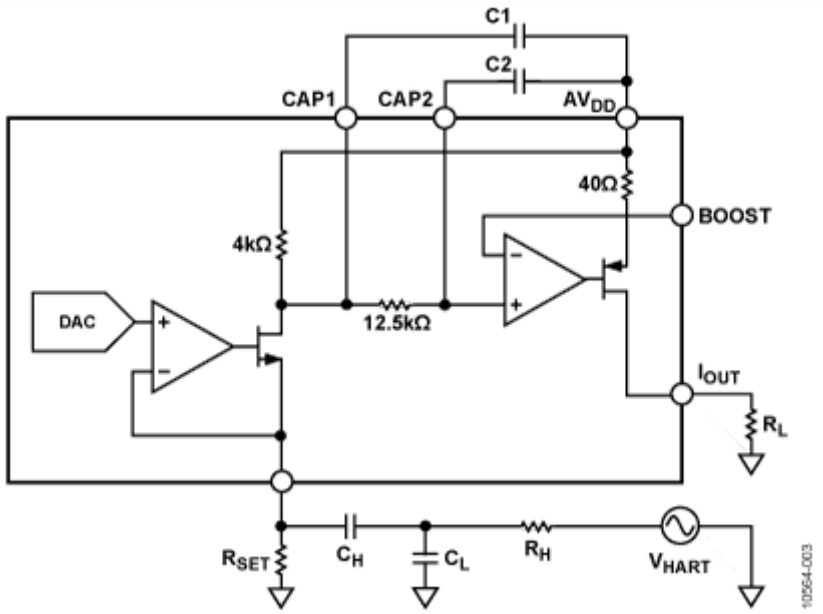
C1 和 C2 可配合器件的数字压摆率控制功能使用，以控制 AD5420 的 IOUT 信号的压摆率。确定电容的绝对值时，要确保调制解调器的 FSK 输出无失真通过。因此，调制解调器输出信号的带宽必须通过 1200 Hz 和 2200 Hz 频率。图 3 显示了实现此要求的电路。在此情况下 C2 保持开路。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 3. AD5420/AD5410 AND AD5700 HART MODEM CONNECTION

图 3. AD5420/AD5410 和 AD5700 HART 调制解调器连接



Enlarge

放大

The low-pass and high-pass filter circuitry is formed through the interaction of R_H, C_L, C_H, and C1, along with some internal circuitry in the AD5420. In calculating the values of these components, the low-pass and high-pass frequency cutoff point targets were >10 kHz and <500 Hz, respectively. Figure 4 shows a plot of the simulated frequency response, while Table 1 shows the effect on the frequency response of increasing each component while the remaining component values are kept constant.

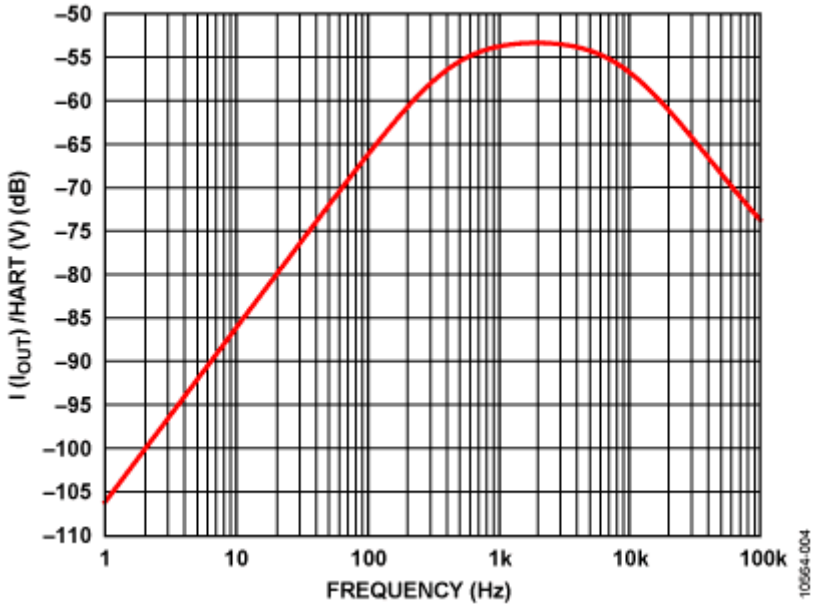
低通和高通滤波器电路通过 R_H、C_L、C_H 和 C1 的相互作用并配合 AD5420 的一些内部电路来形成。在计算这些元件的值时，低通和高通频率截止点目标分别为>10 kHz 和<500 Hz。图 4 显示了仿真频率响应的曲线图，表 1 显示了增加各元件而剩余元件值保持恒定对频率响应的影响。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 4. SIMULATED FREQUENCY RESPONSE

图 4. 仿真频率响应



Enlarge

放大

Table 1. Effect on Frequency Response of Individual

表 1. 个别频率响应的影响

Component Value Increase

元件值增加

Component 元件	C1	CH	CL	RH
fL (Hz)	↓	↓	↓	↓
fH (kHz)	↓	No change 无变化	No change 无变化	No change 无变化
G (dB)	↓	↑	↓	↓

The output of the modem is an FSK signal consisting of 1200 Hz and 2200 Hz shift frequencies. This signal must translate to a 1 mA peak-to-peak current signal. To achieve this, the signal amplitude at the RSET pin must be attenuated. This is due to the internal current gain configuration in the AD5420 design. Assuming that the modem output amplitude is 500 mV peak-to-peak, its output must be attenuated by 500/150 = 3.33. This attenuation is achieved by means of R_H and C_L.

调制解调器的输出是一个 FSK 信号，包括 1200 Hz 和 2200 Hz 移频。这个信号必须转换为 1 mA 峰峰值电流信号。为此，RSET 引脚上的信号幅度必须衰减。这是因为 AD5420 采用内部电流增益配置设计。假定调制解调器的输出幅度为 500 mV 峰峰值，则其输出必须经过 500/150 = 3.33 倍衰减。此衰减通过 R_H 和 C_L 来实现。

The measurements in this circuit note were completed using the following component values:

本电路笔记中的测量使用以下元件值完成：

- C1 = 4.7 nF
- C1 = 4.7 nF
- R_H = 27 kΩ
- R_H = 27 kΩ
- C_L = 4.7 nF
- C_L = 4.7 nF
- C_H = 8.2 nF
- C_H = 8.2 nF

Figure 5 shows the individual 1200 Hz and 2200 Hz shift frequencies measured across a 500 Ω load resistor. Channel 1 shows the modulated HART signal coupled into the AD5420 output (set to output 4 mA), while Channel 2 shows the AD5700 TXD signal.

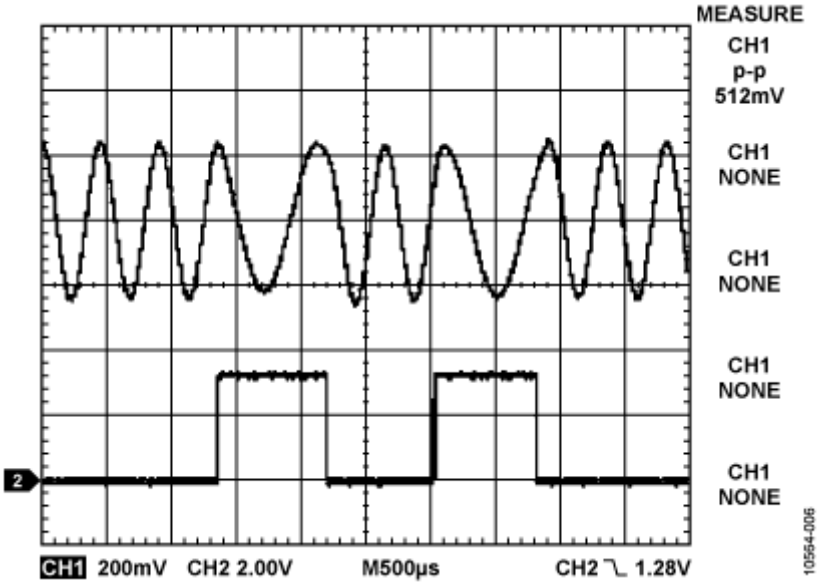
图 5 表明在 500 Ω 负载电阻上分别测得了 1200 Hz 和 2200 Hz 移频。通道 1 显示耦合至 AD5420 输出中的调制 HART 信号（设置为输出 4 mA），而通道 2 显示 AD5700 TXD 信号。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 5. FSK WAVEFORMS MEASURED ACROSS A 500 Ω LOAD

图 5. 在 500 Ω 负载上测得的 FSK 波形



Enlarge

放大

HART Compliance

HART 兼容性

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are numerous physical layer specifications included in the HART specification documents. The two that are most important in this case are the output noise during silence and the analog rate of change.

图 1 中的电路要与 HART 兼容，必须符合 HART 物理层规范。HART 规范文档中包含了众多物理层规范。其中最重要的两个是静默期间的输出噪声和模拟变化率。

Output Noise During Silence

静默期间的输出噪声

When a HART device is not transmitting (silent), it should not couple noise onto the network in the HART extended frequency band. Excessive noise may interfere with reception of HART signals by the device itself or other devices on the network.

当 HART 设备没有进行传输（静默）时，不应在 HART 扩展频带中将噪声耦合到网络上。噪声过高可能会干扰设备本身或网络上的其它设备对 HART 信号的接收。

The voltage noise measured across a 500 Ω load must contain no more than 2.2 mV rms of combined broadband and correlated noise in the extended frequency band. This noise was measured by connecting the HCF_TOOL-31 filter (available from the HART Communication Foundation) across the 500 Ω load and by connecting the output of the filter to a true rms meter (see Figure 6). An oscilloscope was also used to examine the output waveform peak-to-peak voltage.

对于在 500 Ω 负载上测得的电压噪声，其包含的扩展频带中的宽带噪声和相关噪声总和不能超过 2.2 mV（有效值）。此噪声通过在 500 Ω 负载上连接 HCF_TOOL-31 滤波器（可从 HART 通信基金会获得）并将滤波器输出连接到真均方根测量仪（参见图 6）来测量。也可使用示波器来检查输出波形峰峰值电压。

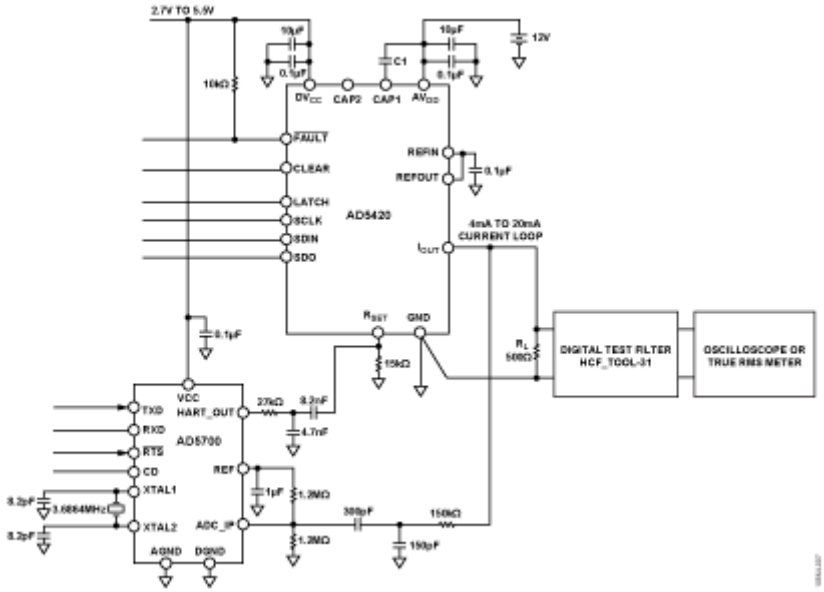
The AD5420 output current was set to 4 mA, 12 mA, and 20 mA. No discernible differences in noise were measured. The rms values measured, with and without the HCF_TOOL-31 band-pass filter, were 115 µV rms and 252 µV rms, respectively. Both of these values are well within the required specifications of 2.2 mV rms (with HART filter) and 138 mV rms (broadband noise without HART filter).

AD5420 输出电流设置为 4 mA、12 mA 和 20 mA。噪声中未测得可辨别的差异。使用和不使用 HCF_TOOL-31 带通滤波器时，测得的均方根值分别为 115 µV rms 和 252 µV rms。这两个值均在要求的 2.2 mV rms（使用 HART 滤波器）和 138 mV rms（不使用 HART 滤波器的宽带噪声）规范内。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

FIGURE 6. HART SPECIFICATIONS TEST CIRCUIT

图 6. HART 规范测试电路



Enlarge

放大

Figure 7 and Figure 8 show the oscilloscope plots for 4 mA and 12 mA output current, respectively. Note that the filter has a pass-band gain of 10. Channel 1 and Channel 2 show the input and output of the filter, respectively.

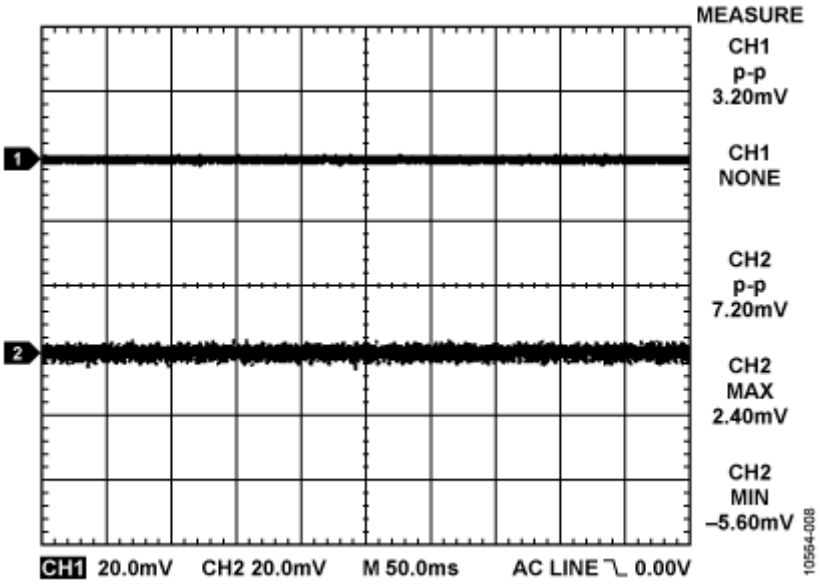
图 7 和图 8 分别显示 4 mA 和 12 mA 输出电流的示波器曲线图。请注意，滤波器的通带增益为 10。通道 1 和通道 2 分别显示滤波器的输入和输出。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 7. NOISE AT INPUT (CH1) AND OUTPUT (CH2) OF HART FILTER WITH 4 MA OUTPUT CURRENT

图 7. HART 滤波器输入（通道 1）和输出（通道 2）端的噪声，输出电流为 4 MA



Enlarge

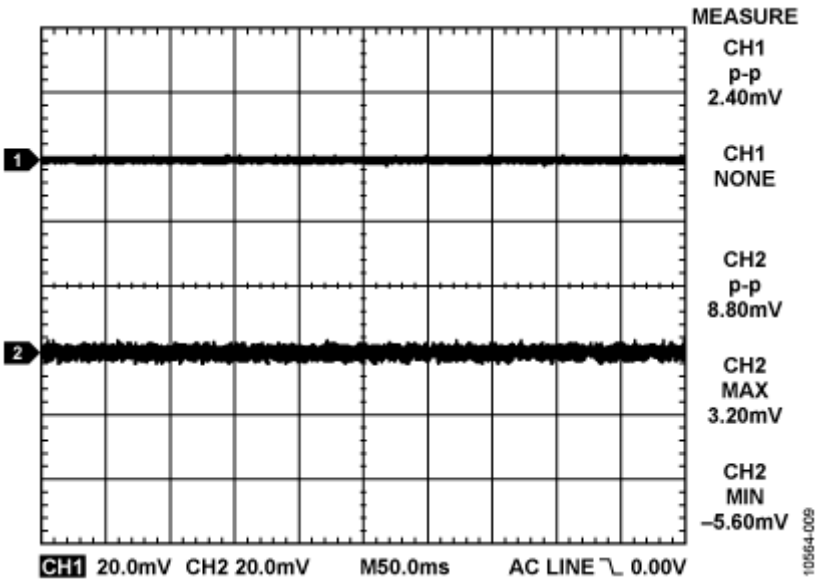
放大

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 8. NOISE AT INPUT (CH1) AND OUTPUT (CH2) OF HART FILTER WITH 12 MA OUTPUT CURRENT

图 8. HART 滤波器输入（通道 1）和输出（通道 2）端的噪声，输出电流为 12 MA



Enlarge

放大

Analog Rate of Change

模拟变化率

This specification ensures that when a device regulates current, the maximum rate of change of analog current does not interfere with HART communications.

Step changes in current disrupt HART signaling. The same test circuit shown in Figure 6 was used. For this test, the AD5420 was programmed to output a cyclic waveform, switching from 4 mA to 20 mA with no delay at either value, to ensure the maximum rate of change. To meet the HART specifications, the waveform at the output of the filter must not exhibit a peak voltage greater than 150 mV. Meeting this requirement ensures that the maximum bandwidth of the analog signaling is within the specified dc to 25 Hz frequency band.

这一技术规范可确保当设备调节电流时，模拟电流的最大变化率不会干扰 HART 通信。电流的阶跃变化会扰乱 HART 信号。使用如图 **6** 所示的相同测试电路。为进行这个测试，AD5420 被编程为输出一个 4 mA 至 20 mA 切换的周期波形，该波形在两个值上都没有延迟，以获得最大变化率。为了符合 HART 规范，滤波器输出端的波形的峰值电压不能大于 150 mV。符合这一要求可确保模拟信号的最大带宽处于规定的直流至 25 Hz 频带中。

The normal time for the output of the AD5420 to change from 4 mA to 20 mA is about 10 µs. This is obviously too fast and would cause major disruption to a HART network. To reduce the rate of change, the AD5420 employs two features: connecting capacitors at the CAP1 and CAP2 pins, and an internal digital slew rate control function (refer to the AD5420 data sheet for details).

AD5420 输出从 4 mA 变为 20 mA 的自然时间约为 10 µs。这个速度显然太快，而且会对 HART 网络造成重大破坏。为了降低变化率，AD5420 提供了两种特性：一是在 CAP1 和 CAP2 引脚处连接电容，二是提供数字压摆率控制功能（详情请参考 AD5420 数据手册）。

It requires very large capacitor values at CAP1 and CAP2 to reduce the bandwidth below 25 Hz. The optimum solution is to use a combination of the external capacitors and the digital slew rate control function of the AD5420. The two capacitors, C1 and C2, have the effect of reducing the rate of change of the analog signal; however, not sufficiently enough to meet the specification. Enabling the slew rate control feature offers the flexibility to set the rate of change.

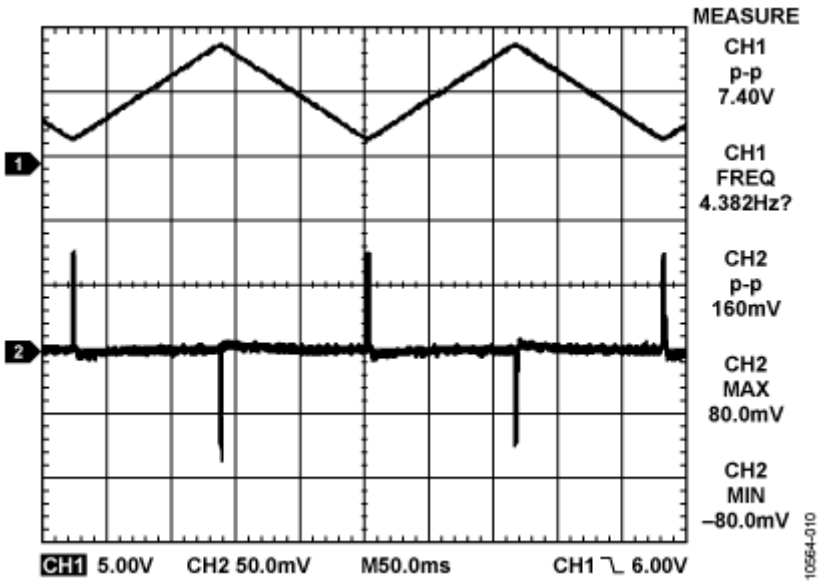
要使带宽降低到 25 Hz 以下，需要在 CAP1 和 CAP2 引脚处连接非常大的电容值。最佳解决方案是结合外部电容和 AD5420 的数字压摆率控制功能。两个电容 C1 和 C2 的作用是降低模拟信号的变化率；不过还不足以满足规范。使能压摆率控制功能可以为变化率的设置提供灵活性。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 9. AD5420 OUTPUT (CH1) AND HART FILTER OUTPUT (CH2), SR CLOCK = 3, SR STEP = 2, C1 = 4.7 NF, C2 = NC

图 9. AD5420 输出（通道 1）和 HART 滤波器输出（通道 2），SR CLOCK = 3，SR STEP = 2，C1 = 4.7 NF，C2 = NC



Enlarge

放大

Figure 9 shows the output of the AD5420 and the output of the HART filter. The peak voltage at the output of the filter is within specification at 80 mV. The slew rate settings are SR CLOCK = 3 and SR STEP = 2, setting the transition time from 4 mA to 20 mA at approximately 120 ms. C1 is 4.7 nF and C2 is unconnected. If this rate of change is too slow, the slew time can be reduced. However, this has the effect of increasing the peak voltage at the output of the filter. The capacitor connected from CAP1 to AV_{DD} can be used to counteract this.

图 9 显示 AD5420 的输出和 HART 滤波器的输出。滤波器输出端的峰值电压为 80 mV，处于规定范围以内。压摆率设置为 SR CLOCK = 3 和 SR STEP = 2，从 4 mA 至 20 mA 的转换时间设为约 120 ms，C1 = 4.7 nF，C2 未连接。如果这个变化率太慢，可以减少压摆时间。但这会使滤波器输出端的峰值电压增加。从 CAP1 连接至 AV_{DD} 的电容可用于抵消此增加。

Figure 10 shows the results of changing the slew rate control settings to SR CLOCK = 5 and SR STEP = 2, while leaving the C1 capacitor value unchanged at 4.7 nF. This results in a transition time of approximately 240 ms. The peak amplitude at the output of the filter can be reduced further by increasing the value of C1, configuring a slower slew rate, or a combination of both.

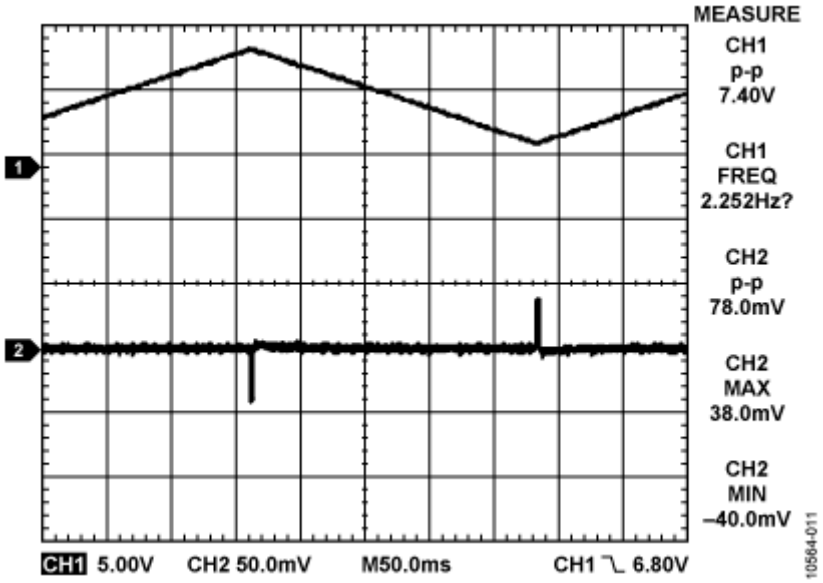
图 10 显示了压摆率控制设置改为 SR CLOCK = 5 和 SR STEP = 2，同时 C1 电容值保持 4.7 nF 不变的结果。这样就会产生约 240 ms 的转换时间。滤波器输出端的峰值幅度可通过增加 C1 值、配置更慢的压摆率或通过两者的组合来进一步降低。

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 10. AD5420 OUTPUT (CH1) AND HART FILTER OUTPUT (CH2), SR CLOCK = 5, SR STEP = 2, C1 = 4.7 NF, C2 = NC

图 10. AD5420 输出（通道 1）和 HART 滤波器输出（通道 2），SR CLOCK = 5，SR STEP = 2，C1 = 4.7 NF，C2 = NC



Enlarge

放大

Transient Voltage Protection

瞬变电压保护

The AD5420 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5420 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as shown in Figure 1. The constraint on the resistor value, (shown in Figure 1 as 18 Ω), is that during normal operation, the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} − 2.5 V, and the two protection diodes and resistor must have appropriate power ratings. With 18 Ω, for a 4 mA to 20 mA output, the compliance limit at the terminal is decreased by V = I_{MAX} × R = 0.36 V. Further protection can be provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors, and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. It is recommended that all remotely connected nodes be protected.

AD5420 内置 ESD 保护二极管，可防止器件在一般工作条件下受损。但是，工业控制环境会使 I/O 电路遭受高得多的瞬变。为了防止过高瞬态电压影响 AD5420，可能需要外部功率二极管和浪涌电流限制电阻，如图 **1** 所示。对电阻值的约束条件（图 1 中显示为 18 Ω）是，在正常工作期间，I_{OUT} 的输出电平必须保持在其顺从电压限值（AV_{DD} − 2.5 V）以内，并且这两个保护二极管和电阻必须具有适当的额定功率。在 18 Ω 下，对于 4 mA 至 20 mA 输出，引脚上的顺从限值降低 V = I_{MAX} × R = 0.36 V。通过瞬态电压抑制器(TVS)或瞬态吸收器可实现进一步的保护。这些元件包括单向和双向抑制器，可提供各种各样的隔离和击穿电压额定值。TVS 应尽量采用最低击穿电压定标，同时在电流输出的功能范围内不导通。建议保护所有远程连接节点。

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The *i*Coupler family of products from Analog Devices, Inc., provides voltage isolation in excess of 2.5 kV. Further information on *i*Coupler products is available at www.analog.com/icouplers. To reduce the number of isolators required, nonessential signals, such as CLEAR, can be connected to GND; FAULT and SDO can be left unconnected, reducing the isolation requirements to only three signals. However, note that eitherFAULT or SDO are required to provide access to the fault detection features of the AD5420.

在许多过程控制应用中，需要在控制器与受控单元之间提供一个隔离栅，以保护和隔离控制电路遭受可能发生的任何危险共模电压。ADI 公司的 *i*Coupler 系列产品可提供超过 2.5 kV 的电压隔离。有关 *i*Coupler 产品的更多信息，请访问 www.analog.com/icouplers。为了减少所需隔离器的数量，CLEAR 等非关键信号可以连到 GND；FAULT 和 SDO 可以不连接，从而只需要隔离三个信号。不过请注意，FAULT 或 SDO 引脚是访问 AD5420 的故障检测功能所必需的。

back to top

返回页首

COMMON VARIATIONS

常见变化

A common variation on the circuit shown in Figure 1 is to use the AD5422 (LFCSP version), which is similar to the AD5420, but has a voltage output channel as well as a current output channel. Circuit Note CN-0065 provides extra information on an IEC 61000 compliant solution for a fully isolated output module using the AD5422 and the ADuM1401 digital isolator. Circuit Note CN-0233 contains information on providing power and data isolation using the ADuM3471 PWM controller and transformer driver with quad-channel isolators.

图 1 所示电路的一个常见变化是使用 AD5422（LFCSP 版本），它类似于 AD5420，但具有电压输出通道和电流输出通道。电路笔记 CN-0065 提供有关 IEC 61000 兼容解决方案的额外信息，该解决方案适合使用 AD5422 和 ADuM1401 数字隔离器的全隔离式输出模块。电路笔记 CN-0233 包含有关提供电源和数据隔离的信息，使用 ADuM3471 PWM 控制器和具有四通道隔离器的变压器驱动器。

If multiple channels are required, the AD5755-1 quad voltage and current output DAC may be used. This product has innovative on-chip dynamic power control that minimizes package power dissipation in current mode. Each channel has a corresponding CHART pin so that HART signals can be coupled to the current output of the AD5755-1.

如果需要多个通道，可使用 AD5755-1 四通道电压和电流输出 DAC。该产品具有创新型片内动态电源控制功能，在电流模式下，可以最大限度地降低封装功耗。各通道均有一个相应的 CHART 引脚，因此 HART 信号可以耦合到 AD5755-1 的电流输出端。

The AD5421 and the AD5700 HART modem can be combined if the requirement is a loop-powered 4 mA to 20 mA HART solution.

如果需要环路供电的 4 mA 至 20 mA HART 解决方案，可以组合 AD5421 和 AD5700 HART 调制解调器。

back to top

返回页首

CIRCUIT EVALUATION AND TEST

电路评估与测试

To build this circuit, it requires the use of the AD5420 evaluation board (EVAL-AD5420EBZ) and the AD5700-1 evaluation board (EVAL-AD5700-1EBZ), see Figure 11. As well as the two evaluation boards, the circuit also requires three external capacitors (C1, C_H, and C_L), a resistor (R_H), a load resistor (R_L), and a UART interface.

要构建此电路，需要使用 AD5420 评估板(EVAL-AD5420EBZ)和 AD5700-1 评估板(EVAL-AD5700-1EBZ)，参见图 11。除外两个评估板，该电路还需要三个外部电容（C1、C_H 和 C_L）、一个电阻(R_H)、一个负载电阻(R_L)和一个 UART 接口。

Equipment Needed

设备要求

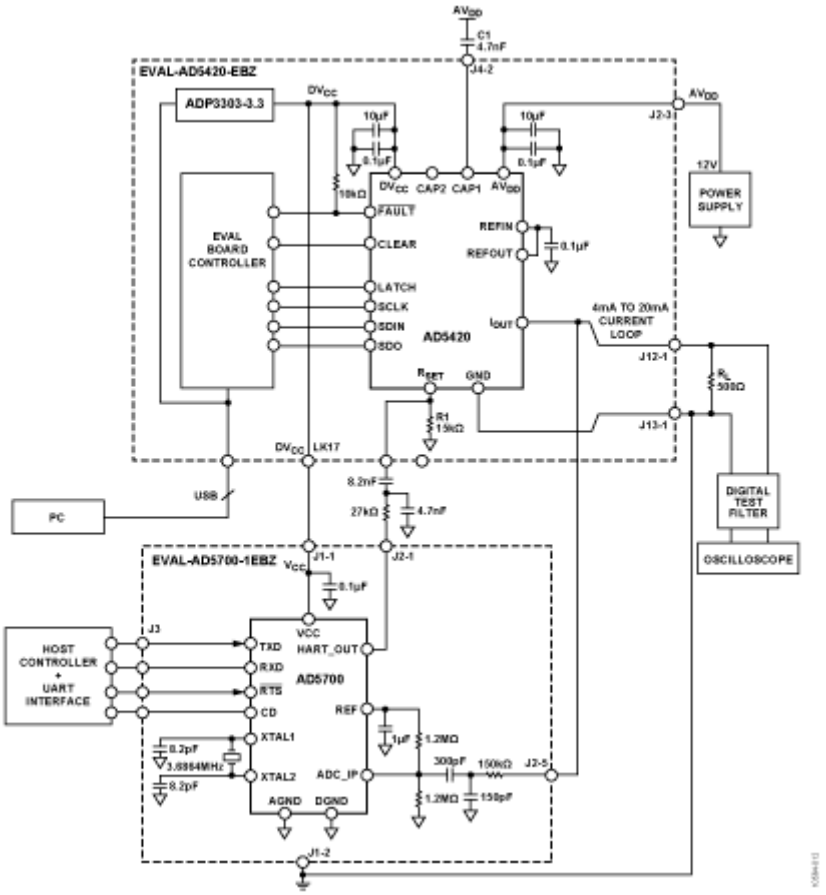
- AD5420 Evaluation Board (EVAL-AD5420EBZ)
- AD5420 评估板(EVAL-AD5420EBZ)
- AD5700 Evaluation Board (EVAL-AD5700-1EBZ)
- AD5700 评估板(EVAL-AD5700-1EBZ)
- PC running Windows® XP with USB port
- 运行 Windows® XP 的 PC，带 USB 端口
- Host controller and UART interface (standard microcontroller, for example, ADuC7060).
- 主机控制器和 UART 接口（标准微控制器，例如 ADuC7060）
- Power supply, 10.8 V to 60 V
- 电源电压：10.8 V 至 60 V
- Digital test filter (HCF_TOOL-31 available from the HART Communication Foundation)
- 数字测试滤波器（HCF_TOOL-31，可从 HART 通信基金会获得）
- Load resistor, 500 Ω
- 500 Ω 负载电阻
- External capacitors, C1 (4.7 nF), CH (8.2 nF), CL (4.7 nF); and a resistor, R_H (27 kΩ)
- 外部电容，C1 (4.7 nF)、CH (8.2 nF)、CL (4.7 nF)；一个电阻，R_H (27 kΩ)
- Oscilloscope, Tektronix DS1012B or equivalent
- 示波器，Tektronix DS1012B 或等效器件

COMPLETE 4 MA TO 20 MA HART SOLUTION (CN0270)

完整 4 MA 至 20 MA HART 解决方案(CN0270)

FIGURE 11. TEST SETUP BLOCK DIAGRAM

图 11. 测试设置框图



Enlarge

放大

For the output noise during silence tests, as described previously, the AD5700 modem was not transmitting (silent). The AD5420 was set to output the required current and passed through the HCF (HART Communication Foundation) band-pass filter. The output noise was then measured using a Tektronix TDS1012B oscilloscope.

对于静默测试期间的输出噪声，如上所述，AD5700 调制解调器并非发射数据（静默）。AD5420 设置为输出所需的电流并通过 HCF（HART 通信基金会）带通滤波器。接着使用 Tektronix TDS1012B 示波器测量输出噪声。

The analog rate of change specification ensures that when the AD5420 regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling.

模拟变化率规范可确保当 AD5420 调节电流时，模拟电流的最大变化率不会干扰 HART 通信。电流的阶跃变化会扰乱 HART 信号。

For this test, the AD5420 was programmed to output a cyclic waveform switching from 4 mA to 20 mA with no delay at either value to ensure the maximum rate of change. The slew rate settings used were SR CLOCK = 3 and SR STEP = 2, with C1 set to 4.7 nF and C2 open circuit. Measurements were also

completed whereby the slew rate was reduced even further by changing the SR CLOCK setting to 5 rather than 3 and leaving all other settings and component values unchanged.

为进行这个测试，AD5420 被编程为输出一个 4 mA 至 20 mA 切换的周期波形，该波形在两个值上都没有延迟，以获得最大变化率。所用的压摆率设置为 SR CLOCK = 3 和 SR STEP = 2，C1 设置为 4.7 nF，C2 保持开路。同时完成测量，以便将 SR CLOCK 设置改变为 5 而不是 3，并保持所有其他设置和元件值不变，从而进一步降低压摆率。

back to top

返回页首

LEARN MORE

了解详情

CN0270 Design Support Package:

CN0270 设计支持包：

http://www.analog.com/CN0270-DesignSupport

http://www.analog.com/CN0270-DesignSupport

Maurice Egan, *Configuring the AD5420 for HART Communication Compliance*, Application Note AN-1065, Analog Devices.

Maurice Egan，*AD5420 的 HART 通信兼容配置*，应用笔记 AN-1065，ADI 公司。

HART Communication Foundation

HART 通信基金会

Data Sheets and Evaluation Boards

数据手册和评估板

AD5420 Data Sheet and Evaluation Board

AD5420 数据手册和评估板

AD5700 Data Sheet and Evaluation Board

AD5700 数据手册和评估板

AD5700-1 Data Sheet and Evaluation Board

AD5700-1 数据手册和评估板

REVISION HISTORY

修订历史

5/12—Rev. 0 to Rev. A

2012 年 5 月—修订版 0 至修订版 A

4/12—Revision 0: Initial Version

2012 年 4 月—修订版 0：初始版